White Paper

Using a Rad Hard Switching Regulator as a VTT Terminator in DDR Applications

Introduction

DDR memory is becoming increasingly popular in satellite and space applications. Currently, however, no power solution can survive the harsh environments of space while meeting the power requirements of the VTT rail. This paper introduces the ISL70003SEH, a radiation hardened sync buck regulator, as a solution to the VTT termination regulator. It explains the modifications needed to generate the V_{REF} voltage and track the VDDQ rail. Performance of Intersil's rad hard switching regulator ISL70003SEH is also demonstrated.

DDR Memory

DDR SDRAM, due to its advantages over standard SDRAM, is utilized in PC applications, graphic cards, blade servers and networking and communication devices. These same advantages have made DDR memory an enabling technology in space applications. DDR memory utilizes both the rising and falling edge of the clock signal to transmit data, essentially doubling the transfer data rate for a given clocking frequency, which allows for faster processing of large amounts of data. In addition, each new generation of DDR memory doubles the transfer rate of its predecessor. DDR memory features an active termination scheme called stub series termination logic (SSTL), which improves noise immunity and power supply rejection (see Figure 1). DDR also benefits from a reduction in overall power consumption through the use of lower operating voltages compared to SDRAM. Table 1 compares the max transfer speed and operating voltage of the SDRAM versus DDR memory.

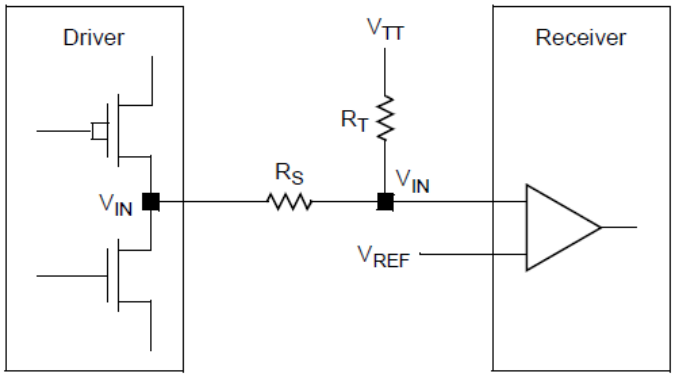

Figure 1. SSTL Termination Scheme in DDR Memory

Table 1. Comparison of SDRAM and DDR Memory Speed and Supply Rail(s)

	SDRAM	DDR1	DDR2	DDR3
Nominal Supply Voltage (s)	3.3V	VDDQ = 2.5V VTT = VDDQ/2 V_{REF} = VDDQ/2	VDDQ = 1.8V VTT = VDDQ/2 V_{REF} = VDDQ/2	VDDQ = 1.5V VTT = VDDQ/2 V_{REF} = VDDQ/2
Max Data Rate	100Mbit/s	400Mbit/s	800Mbit/s	1.6Gbit/s
JEDEC Interface	LVTTL	SSTL_2	SSTL_18	SSTL_15

Power Requirements

There are three voltages that need to be generated and regulated in a DDR memory system: VDDQ, V_{REF} and VTT. VDDQ is used to power the memory controller, the I/O banks and other circuitry such as the clock synthesizer. V_{REF} is a low power reference source that tracks the middle point of VDDQ. It is the threshold voltage of the differential receiver and is usually provided by a buffered resistor divider. VTT is the voltage source that powers the parallel termination resistors. This third power source also has to track the middle point of the VDDQ voltage over voltage, temperature and noise. The current flow direction of the VTT power source changes as the state of the bus changes. Thus, VTT needs to both sink current and source current as illustrated in Figure 2.

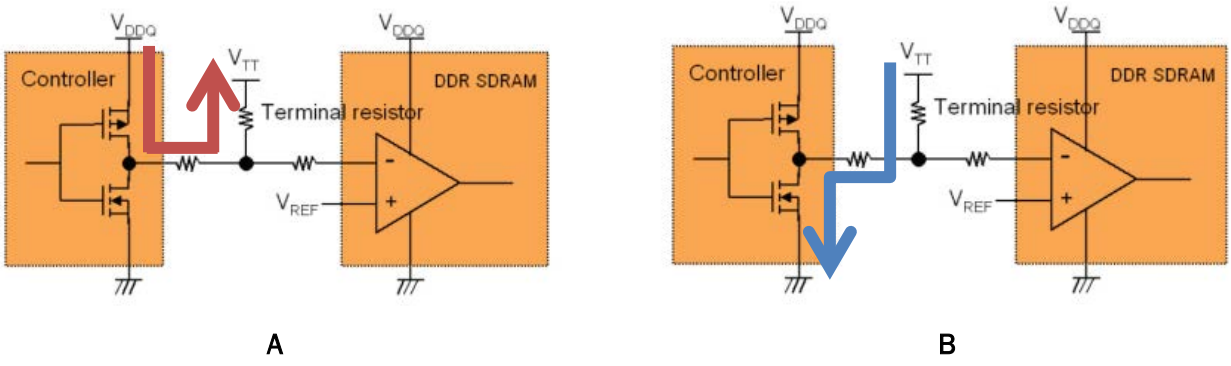

Figure 2. (A) VTT Regulator Sinking Current During HI State
(B) VTT Regulator Sourcing Current During LO State

Couple these stringent power requirements with the ability to operate in the harsh environs of space without any loss of regulation or performance degradation. There is a clear void with regards to a power solution that is suitable as a VTT terminating regulator.

VTT Terminating Regulator Solution

The ISL70003SEH is Intersil's third radiation and single-event effects (SEE) hardened point of load (POL) buck regulator intended for space applications. The ISL70003SEH uses voltage mode control architecture with feed-forward and is capable of operating over an input voltage range of 3.0V to 13.2V. This integrated circuit reduces size and cost by integrating low $R_{DS(on)}$ MOSFETs and switching at a selectable frequency of 500kHz or 300kHz. The regulator has several enhancements that make it a viable solution as a VTT regulator. These include the ability to sink 3A and a high speed buffer amplifier to generate the V_{REF} voltage.

The non-inverting input of the error amplifier is pinned out to provide tracking between the VDDQ and VTT rails.

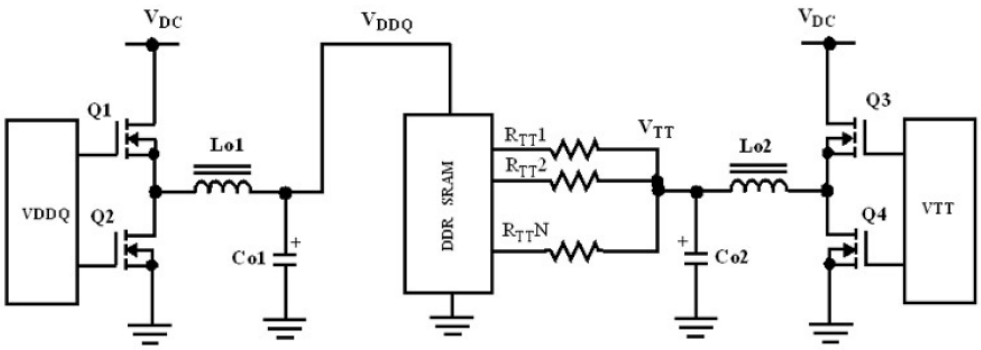

Figure 3. Independent Power Architecture for Power DDR Memory

In the DDR application presented in Figure 3, an independent architecture is implemented to generate the voltages needed for DDR memory applications. Consequently, both VDDQ and VTT are derived independently from the main power source, typically 3.3V or 5V. In the case of DDR1, the first regulator supplies the VDDQ voltage of 2.5V and the second regulator generates the VTT rail equal to VDDQ/2. The VDDQ regulator may be any of Intersil's radiation hardened POL regulators, giving the designer the flexibility to pick a solution that will meet the load requirements. The VTT terminating regulator will be the ISL70003SEH switching regulator. We will now focus on the implementation and performance of the ISL70003SEH in a VTT termination application.

Figure 4 is a simplified schematic demonstrating the connections needed to generate VTT and V_{REF} using the ISL70003SEH. The midpoint of the R/R resistor divider network from VDDQ is connected to both non-inverting inputs of the error amplifier and the buffer amplifier, effectively providing the tracking function required for VTT and V_{REF}. The output of the error amplifier is the input to the PWM comparator that controls the duty cycle of the internal MOSFETs, which generates VTT after the LC low pass filter. VTT is connected to the inverting input of the error amplifier, which is essentially configured in a unity gain. Blocks Z_{IN} and Z_{FB} is the external compensation network needed to stabilize the regulator.

The output of the buffer is tied back to the inverting input for unity gain configuration. The buffer output voltage serves as a 1.25V reference (V_{REF}) for the DDRI memory chips. Sourcing capability of the buffer amplifier is 10mA typical (20mA max) and needs a minimum of 1µF load capacitance for stability.

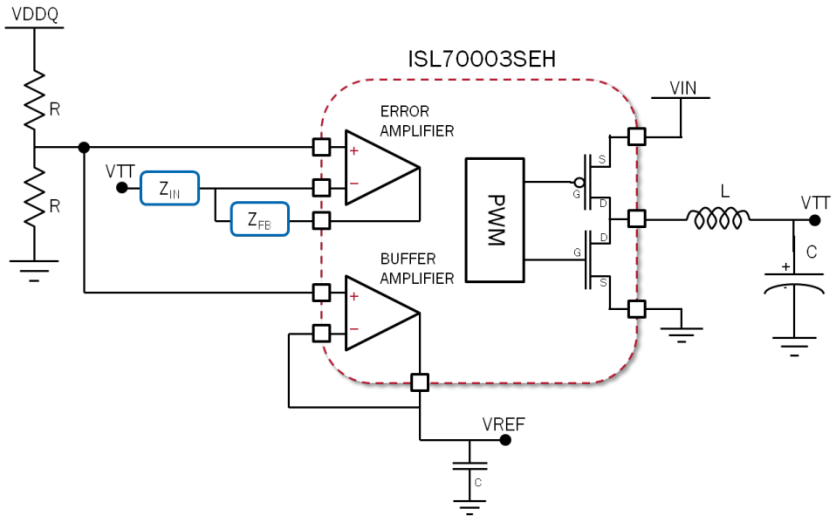

Figure 4. Simplified VTT Regulator

At start up, in order for the ISL70003SEH to properly track the VDDQ voltage, the soft-start capacitor on the ISL70003SEH should be two to three times lower than the soft-start capacitor on the VDDQ regulator. This allows the VDDQ regulator voltage to be the lowest input into the error amplifier of the VTT regulator and dominate the soft-start ramp. Diode emulation mode must be disabled to ensure that the regulator sinks the current. At lower input voltages (e.g., 3.3V) the VDDQ/2 value is higher than the common mode range of the error amplifier and buffer amplifier, therefore certain applications such as DDRI and DDRII cannot be implemented unless the input voltage is raised to 5V. For a 3.3V input voltage only DDRIII may be implemented.

The ISL70003SEH sync buck regulator must provide excellent performance to meet the regulation requirements of the VTT rail. The following example depicts one of the stringent requirements for DDR power solutions and how the ISL70003SEH can meet and exceed the imposed regulations. In the case of DDRI, VTT must equal V_{REF} ± 40mV at all times including DC offsets and transient response. The two sources of error in DC are the offset voltages of the error and buffer amplifier. These offset voltages are specified over temperature and radiation to be 3mV and 4mV maximum for the error amplifier and the buffer amplifier, respectively. Subtracting the DC errors from the 40mV tolerance results in a maximum allowable deviation of 33mV for transient response, which is 2.7% of the 1.25V VTT rail.

Table 2. DDRI Maximum Voltage Limits

Parameter	Min	Typical	Max	Unit
VDDQ	2.3	2.5	2.7	V
V_{REF}	1.13	1.25	1.38	V
VTT	V_{REF} - .04	V_{REF}	V_{REF} + .04	V

Using Table 2 and assuming 25Ω as series (RS) and termination (RT) termination resistors in Figure 1, it's fairly easy to calculate the maximum current which the VTT rail will source and sink. The VTT rail would sink:

$(VDD_{max} - VTT_{min})/(RT + RS + RDR) = (2.7 - 1.11)V / (25 + 25 + 10)\Omega = 26.5mA$

The VTT rail would source:

$VTT_{max} / (RT + RS + RDR) = 1.39V / (25 + 25 + 10)\Omega = 23.2mA$

RDR is the driver on resistance that would vary by manufacturer, but common values range from 10Ω to 40Ω. At first glance, the load demand may not seem high and with a balanced number of high and low signals the average current required would be close to zero. However, a bus that had all DDR signals low (+115 signals) would cause a transient current demand of approximately 2.7 A.

Figure 5 shows the transient response of the ISL70003SEH when a 3A load step is applied using the evaluation board. The load step from -1.5A to 1.5A causes a deviation of 20mV on the VTT rail and load release from 1.5A to -1.5A induces a voltage transient of 25mV on the VTT rail. The regulator's dynamic response is more than capable of meeting the requirements to keep the VTT rail within specification.

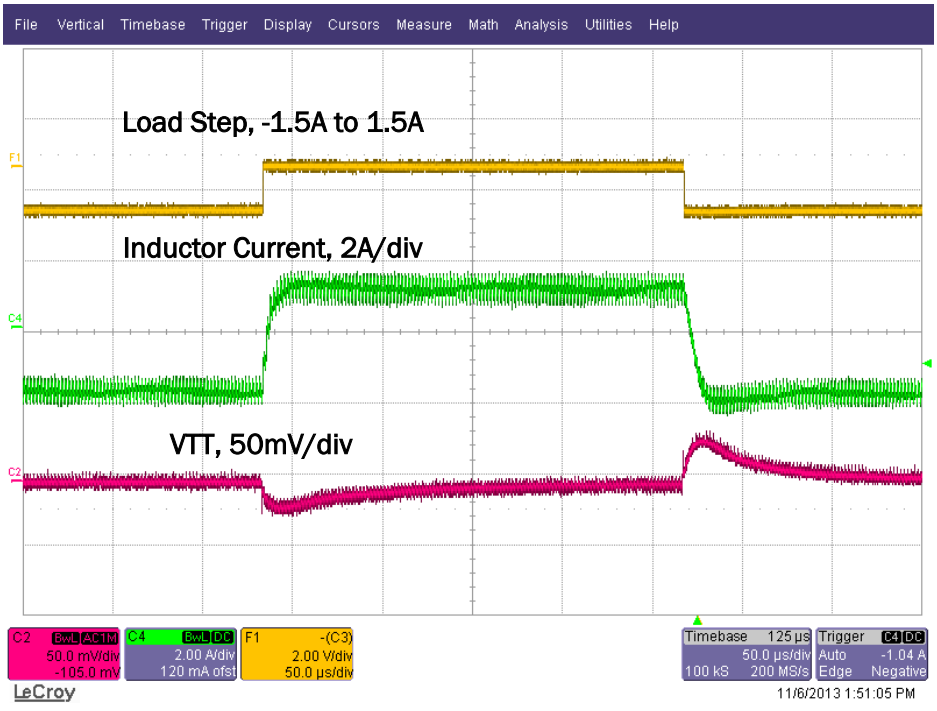

Figure 5. VTT Transient Response -1.5A to 1.5A.

The ISL70003SEH switching regulator is specified at total dose (TID) ratings of 100krad(Si) at high dose rate (50-300 rad(Si)/s) and of 50krad(Si) at low dose rate (< 0.01 rad(Si)/s), as specified by MIL-STD-883 test method 1019. The part is acceptance tested on a wafer-by-wafer basis to 50krad(Si) at low dose rate and to 100krad(Si) at high dose rate. The ISL70003SEH is also single-event effects rated for both destructive and nondestructive effects to a linear energy transfer (LET) value of 86.4MeV.cm^2/mg. Both radiation performance and the SEE rating are more than adequate for space applications.

Conclusion

The advantages of DDR memory over SDRAM can now be realized in satellite applications. The ISL70003SEH is Renesas' third generation POL buck regulator for space applications. Its enhanced power management features allow the regulator to be used in DDR applications and is especially suited for the VTT termination rail. With the superior performance over low and high dose radiation exposure and the overall robust capability of the ISL70003SEH, the solution guarantees class leading performance over any mission life. What's more, no additional spot shielding, radiation lot acceptance testing, or other techniques are required to get this assurance. Find out more about Renesas' space and harsh environment solutions at https://www.renesas.com/products/space-harsh-environment.html.

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